WHAT IS CLAIMED IS:

1. A memory arbiter, comprising:

a memory area; and

a memory controller coupled to the memory area, wherein the memory controller is configured to receive memory requests and corresponding priorities from a microprocessor, and wherein the memory controller is configured to continue to service current lower priority requests for a predefined period if an incoming higher priority request is directed to a same page of memory as the current lower priority requests.

2. The memory arbiter of claim 1, wherein the memory controller is configured to continue servicing any requests from a same agent as the lower priority request during the predefined period.

3. The memory arbiter of claim 1, wherein the memory controller is configured to process the incoming high priority request after the predefined period expires.

4. The memory arbiter of claim 3, wherein the memory controller is configured to eventually resume servicing any lower priority requests after the high priority request is processed.

5. The memory arbiter of claim 1, further comprising:

a counter to monitor the predefined period.

6. A method for servicing data in a computer system, comprising:

receiving a first memory request;

servicing the first memory request;

receiving a second memory request having a priority greater than the first memory request; and

continuing to process the first memory request for a predefined period if the second memory request is directed to a same page of memory as the first memory request.

7. The method of claim 6, further comprising:

continuing to process any request from a same agent as the first memory request during the predefined period.

8. The method of claim 7, further comprising:

servicing the second memory request after the predefined period expires.

9. The method of claim 8, further comprising:

resume eventually servicing the any lower priority requests after the higher priority request is processed.

10. A computer system, comprising:

a processor to initiate higher and lower priority memory requests;

a memory area; and

a memory controller coupled to the memory area, wherein the memory controller is configured to receive memory requests and corresponding priorities from the processor, and wherein the memory controller is configured to continue to service current lower priority requests for a predefined period if an incoming higher priority request is directed to a same page of memory as the current lower priority requests.

11. The computer system of claim 10, wherein the memory controller is configured to continue servicing any requests from a same agent as the lower priority request during the predefined period.

12. The computer system of claim 10, wherein the memory controller is configured to process the incoming high priority request after the predefined period expires.

13. The computer system of claim 12, wherein the memory controller is configured to eventually resume servicing any lower priority requests after the high priority request is processed.

14. The computer system of claim 10, further comprising:

a counter to monitor the predefined period.

15. A machine readable medium having stored therein a plurality of machine readable instructions executable by processor to service data, comprising:

instructions to receive a first memory request;

instructions to service the first memory request;

instructions to receive a second memory request having a priority greater than the first memory request; and

instructions to continue to process the first memory request for a predefined period if the second memory request is directed to a same page of memory as the first memory request.

16. The machine readable medium of claim 15, further comprising:

instructions to continue to process any request from a same agent as the first memory request during the predefined period.

17. The machine readable medium of claim 15, further comprising:

instructions to service the second memory request after the predefined period expires.

18. The machine readable medium of claim 17, further comprising:

instructions to resume eventually servicing the any lower priority requests after the higher priority request is processed.

19. A memory arbiter, comprising:

a memory area; and

a memory controller coupled to the memory area, wherein the memory controller is configured to receive memory requests and corresponding priorities from a microprocessor, and wherein the memory controller is configured to interrupt servicing of higher priority requests after a predefined number are processed to process lower priority requests for a predefined period of time.

20. The memory arbiter of claim 19, wherein the memory controller is configured to redefine the status of the higher priority requests to a lower priority status after a predefined number are processed.

21. The memory arbiter of claim 19, wherein the memory controller is configured to reinstate the higher priority requests to it's initial priority status after the lower priority request is processed.

22. The memory arbiter of claim 19, wherein the memory controller is configured to resume servicing higher priority requests after the predefined period expires.

23. The memory arbiter of claim 19, further comprising:
a counter for monitoring the number of high priority requests.

24. A method to service data in a computer system, comprising:
receiving and servicing a plurality of high priority memory requests;
receiving one or more memory requests having lower priority than the plurality of higher priority memory requests; and
interrupting servicing of higher priority requests after a predefined number is processed to process one or more lower priority requests for a predefined period of time.

25. The method of claim 24, further comprising:
redefining the status of the higher priority requests to a lower priority status after a predefined number are processed.

26. The method of claim 24, further comprising:
reinstating the higher priority requests to an initial priority status after the lower priority requests is processed.

27. The method of claim 24, further comprising:

resuming servicing higher priority requests after the predefined period expires.

28. A computer system, comprising:

a processor for initiating a higher and lower priority memory requests;

a memory area; and

a memory controller coupled to the memory area, wherein the memory controller is configured to receive memory requests and corresponding priorities from the processor, and wherein the memory controller is configured to interrupt servicing of higher priority requests after a predefined number is processed to process one or more lower priority requests for a predefined period of time.

29. The computer system of claim 28, wherein the memory controller is configured to redefine the status of the higher priority requests to a lower priority status after a predefined number are processed.

30. The computer system of claim 28, wherein the memory controller is configured to reinstate the higher priority requests to it's initial priority status after the lower priority request is processed.

31. The computer system of claim 28, wherein the memory controller is configured to resume servicing higher priority requests after the predefined period expires.

32. The computer system of claim 28, further comprising:

a counter to monitor the number of high priority requests.

33. A machine readable medium having stored therein a plurality of machine readable instructions executable by a processor to service data, comprising:

instructions to receive and service a plurality of high priority memory requests;

instructions to receive one or more memory requests having lower priority than the plurality of higher priority memory requests; and

instructions to interrupt servicing of higher priority requests after a predefined number are processed to process one or more lower priority requests for a predefined period of time.

34. The method of claim 33, further comprising:

instructions to redefine the status of the higher priority requests to a lower priority status after a predefined number are processed.

35. The method of claim 33, further comprising:

instructions to reinstate the higher priority requests to an initial priority status after the lower priority requests are processed.

36. The method of claim 33, further comprising:

instructions to resume servicing higher priority requests after the predefined period expires.